BEE 271 Spring 2017
Homework 5

Please answer the following questions. Each is worth 8 points.

1. Draw a state table for an SR latch and a circuit for one using NAND gates.

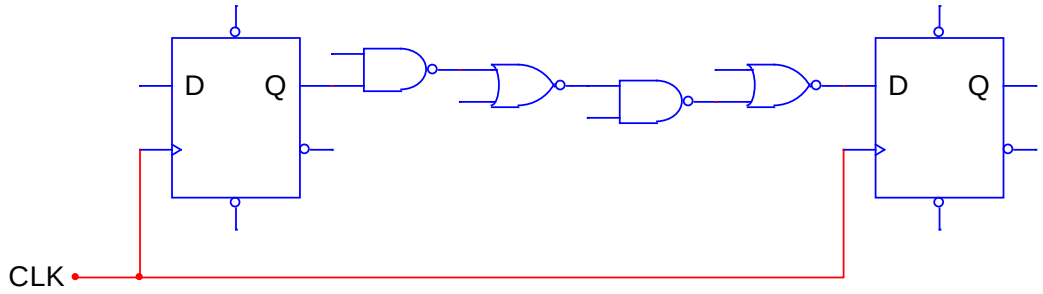
2. Draw a circuit for a gated latch using NAND gates.

3. What is the difference between a latch, a gated latch, and master-slave and edge-triggered flip-flop? Draw the schematic symbols for each.

4. What do the terms positive and negative edge-triggered mean?

5. What is setup time? What is hold time?

6. Referring to the following circuit fragment, assume this represents the critical path in an actual circuit where the rest of the pins have sensible inputs and that t_{su} = 0.4 ns, t_h = 0.2 ns, 0.4 ns ≤ t_{cQ} ≤ 0.5 ns and t_{gate} = 0.5 ns. What is T_{min}, the minimum clock period?



7. Draw a truth table for a JK flip-flop, showing Q(t+1) for the various combinations of J and K and create a JK flip-flop using a D flip-flop.

8. What is the difference between the = and <= operators in Verilog?

9. Write a Verilog module that implements a JK flip-flop with an *asynchronous* reset.

10. Create a 3-bit counter in Verilog that cycles through this sequence, 3, 5, 4, 2, 0, 6, 1, 7, with a synchronous reset to 4.

11. What is the difference between a Mealy and a Moore design? Draw a picture of each.

12. Create a Verilog module that implements an 8-bit 2's complement up/down counter with a *synchronous* reset to zero and a special feature: It should not overflow. If it's counting up and it hits the max positive, it should stay at that count and not roll over into a negative number. Similarly when counting down, if it hits the max negative, it should stay at that value.